THAT WHICH IS CLAIMED:

1. An integrated circuit device, comprising:

first and second complementary data line pairs disposed on a substrate and extending along a first direction, the first and second complementary data line pairs arranged such that first and second data lines of the first complementary data line pair have a first data line of the second complementary data line pair disposed therebetween;

an equalization transistor comprising respective first and second source/drain regions in the substrate that are coupled to respective ones of the first and second data lines of the first complementary data line pair and an equalization transistor gate electrode disposed on the substrate between the first and second data lines of the first complementary data line pair;

a first precharge transistor comprising the first source/drain region, a third source/drain region in the substrate displaced from the first source/drain region along the first direction, and a first precharge transistor gate electrode disposed on the substrate between the first and third source/drain regions; and

a second precharge transistor comprising the second source/drain region, a fourth source/drain region in the substrate displaced from the second source/drain region along the first direction, and a second precharge transistor gate electrode disposed on the substrate between the second and fourth source/drain regions; and

a precharge voltage bus conductor on the substrate and electrically coupled to the third and fourth source/drain regions.

2. A device according to Claim 1:

wherein the first and second source/drain regions underlie the first and second data lines of the first complementary data line pair, respectively; and

wherein the equalization transistor gate electrode comprises a first elongate conductive region disposed between the first and second data lines of the first complementary data line pair.

3. A device according to Claim 2, wherein first elongate conductive region is substantially equidistant from the first and second data lines of the first complementary data line pair.

4. A device according to Claim 2, wherein the first elongate conductive region overlies at least a portion of the first data line of the second complementary data line pair.

5. A device according to Claim 2, wherein the first and second precharge transistor gate electrodes comprise a second elongate conductive region extending along a second direction transverse to the first direction and disposed between the first and third source/drain regions and between the second and fourth source/drain regions.

6. A device according to Claim 5, wherein the first elongate conductive region extends contiguously and substantially perpendicularly from the second elongate conductive region.

7. A device according to Claim 5, wherein the second elongate conductive region and the first and second data lines of the first complementary data line pair cross one another.

8. A device according to Claim 5, wherein the second elongate conductive region and the first and second data lines of the first complementary data line pair do not cross one another.

9. A device according to Claim 5, wherein the precharge voltage bus conductor comprises a conductive line extending along the second direction.

10. A device according to Claim 9, wherein the first complementary data line pair and the precharge voltage bus cross one another.

11. A device according to Claim 9, wherein the first complementary data line pair and the precharge voltage bus do not cross one another.

12. A device according to Claim 5, wherein the first elongate conductive region and the second elongate conductive region form a T-shaped conductive region.

13. A device according to Claim 1, wherein the first and second complementary data line pairs comprise first and second local input/output (I/0) line pairs of a memory circuit.

14. A device according to Claim 1, wherein the first and second complementary data line pairs comprise first and second global input/output (I/0) line pairs of a memory circuit.

15. A device according to Claim 1, wherein the first, second, third and fourth source/drain regions are disposed in a common active region.

16. A device according to Claim 1:

wherein the equalization transistor comprises a first equalization transistor;

wherein the second complementary data line pair comprises a second data line disposed adjacent the second data line of the first complementary data line pair;

wherein the device further comprises:

a conductive line disposed adjacent the second data line of the second complementary data line pair and electrically connected to first data line of the first complementary data line pair;

a second equalization transistor comprising respective fifth and sixth source/drain regions in the substrate that are coupled to respective ones of the second data line of the second complementary data line pair and the conductive line and a second equalization transistor gate electrode disposed on the substrate between the second data line of the second complementary data line pair and the conductive line;

a third precharge transistor comprising the fifth source/drain region, a seventh source/drain region in the substrate displaced from the fifth source/drain region along the first direction, and a third precharge transistor gate electrode disposed on the substrate between the fifth and seventh source/drain regions; and

a fourth precharge transistor comprising the sixth source/drain region, an eighth source/drain region in the substrate displaced from the sixth source/drain region along the first direction, and a fourth precharge transistor gate electrode disposed on the substrate between the sixth and eighth source/drain regions; and

wherein the precharge voltage bus conductor is electrically coupled to the seventh and eighth source/drain regions.

17. A device according to Claim 16, wherein the conductive line is coupled to the first data line of the second complementary data line pair by a jumper that crosses the second data line of the first complementary data line pair and the second data line of the second complementary data line pair.

18. A device according to Claim 16, wherein the conductive line comprises an extension of the first data line of the second complementary data line pair.

19. A device according to Claim 16:

wherein the fifth and sixth source/drain regions underlie the second data line of the second complementary data line pair and the conductive line, respectively; and

wherein the second equalization transistor gate electrode comprises a first elongate conductive region disposed between the second data line of the second complementary data line pair and the conductive line

20. A device according to Claim 19, wherein first elongate conductive region is substantially equidistant from the second data line of the second complementary data line pair and the conductive line.

21. A device according to Claim 19, wherein the first and second complementary data line pairs extend along a first direction, and wherein the third and fourth precharge transistor gate electrodes comprise a second elongate conductive region extending along a second direction transverse to the first direction and disposed between the fifth and seventh source/drain regions and between the sixth and eighth source/drain regions.

22. A device according to Claim 21, wherein the first elongate conductive region extends contiguously and substantially perpendicularly from the second elongate conductive region.

23. A device according to Claim 21, wherein the second elongate conductive region and the second data line of the second complementary data line pair cross one another.

24. A device according to Claim 21, wherein the second elongate conductive region and the second data line of the second complementary data line pair do not cross one another.

25. A device according to Claim 21, wherein the first elongate conductive region and the second elongate conductive region form a T-shaped conductive region.

26. A device according to Claim 16, wherein the first, second, third and fourth source/drain regions are disposed in a common active region.

27. A device according to Claim 16, further comprising:

a third equalization transistor comprising the second and fifth source/drain regions coupled to respective ones of the second data line of the first complementary data line pair and the second data line of the second complementary data line pair and a third equalization transistor gate electrode disposed on the substrate between the second data line of the first complementary data line pair and the second data line of the second complementary data line pair.